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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/536,452	03/28/2000	Ronny Ronen	02207/8754	5160

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/536,452	RONEN ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,7-9,11-15,17,18 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,4,7-9,11,13-15,17,18 and 22* is/are rejected.

7)☒ Claim(s) *12,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4, 7-9, 11-15, 17-18, and 22-24 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 2/23/2005.

Claim Objections

3. Claim 1 is objected to because of the following informalities: Please insert a period at the end of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4, 7-9, 11, 13-15, 17-18, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 (as applied in the previous Office Action and herein referred to as Killian).

6. Referring to claim 1, Killian has taught a processor comprising:

a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.

b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:

(i) means for truncating generated address references of the second bit size to the first bit size. See Fig.5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

(ii) means for determining that the first bit size address space subset is signed address space or unsigned address space based on a setting of an address format control signal, the address format control signal having a first setting to indicate unsigned address space and a second setting to indicate signed address space. When in 32-bit mode, bits in the status register signal to the system whether the 32-bit mode is 32-bit user mode or 32-bit kernel/supervisor mode. See column 17, lines 25-27. With one signal setting (32-bit user mode), the system deals only with unsigned address space (positive addresses). See column 17, line 66, to column 18, line 1. Also, see Fig.3A and note the unsigned address space in 32-bit user mode. With a second signal setting (32-bit kernel/supervisor mode), the system deals with signed address space. See column 19, lines 30-33, and column 3, lines 38-55. That is in kernel/supervisor mode, both user and kernel/supervisor address may be accessed (negative and positive addresses).

(iii) means for extending to the second bit size the truncated generated address references based on results from said means for determining, zero-extending the truncated generated

address references if the first bit size address space is unsigned and sign-extending the truncated generated address references if the first bit size address space subset is signed. See column 17, lines 61-68, and note that in 32-bit user mode (unsigned space), the upper 32-bits are always forced to zero (zero-extension). Furthermore, see column 18, lines 8-17, and note that when in 32-bit kernel/supervisor mode (signed space), addresses are sign-extended. Since, the mode is determined by the status register signal, the type of extension is also determined by the signal.

7. Referring to claim 2, Killian has taught a processor as described in claim 1. Killian has further taught that the first bit size is 32-bit and the second bit size is 64-bit. See column 3, lines 30-31, and column 5, lines 8-19.

8. Referring to claim 4, Killian has taught a processor as described in claim 1. Killian has further taught that the means for confining includes means for generating an address fault. See column 11, lines 3-5. The 32-bit address (which would be represented as an extended 64-bit number in the 64-bit environment) that is used to select a memory location in the address space subset is checked for a certain value and if that value exists, then an address error exception will occur.

9. Referring to claim 7, Killian has taught a processor comprising:

a) a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size. See Fig. 1 and column 7, lines 49-54. Note the existence of main memory and an instruction cache.

b) an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application. See Fig. 1. Note that data and instructions are

retrieved from memory/cache by the EIC (component 25) and propagated along bus 30 to the execution unit.

c) said instruction execution core to determine that the application is confined to a first bit size address space subset. See column 19, lines 36-40.

d) said instruction execution core to generate an address reference of the second bit size as part of execution of the instruction. See column 12, lines 26-65. Also, see Fig.5D and note that a virtual address is generated (at the middle of the page).

e) said instruction execution core to truncate the generated address reference from the second bit size to the first bit size. See Fig.5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

f) said instruction execution core to determine that the first bit size address space subset is signed address space or unsigned address space based on a setting of an address format control flag, the address format control flag having a first setting to indicate unsigned address space and a second setting to indicate signed address space. When in 32-bit mode, bits in the status register signal to the system whether the 32-bit mode is 32-bit user mode or 32-bit kernel/supervisor mode. See column 17, lines 25-27. With one signal setting (32-bit user mode), the system deals only with unsigned address space (positive addresses). See column 17, line 66, to column 18, line 1. Also, see Fig.3A and note the unsigned address space in 32-bit user mode. With a second signal setting (32-bit kernel/supervisor mode), the system deals with signed address space. See column 19, lines 30-33, and column 3, lines 38-55. That is in kernel/supervisor mode, both user and kernel/supervisor address may be accessed (negative and positive addresses).

g) said instruction execution core to zero-extend the truncated, generated address reference to the second bit size if the first bit size address space is determined to be unsigned address space. See column 17, lines 61-68, and note that in 32-bit user mode (unsigned space), the upper 32-bits are always forced to zero (zero-extension).

h) said instruction execution core to sign extend the truncated, generated address reference to the second bit size if the first bit size address space subset is determined to be signed address space. See column 18, lines 8-17, and note that when in 32-bit kernel/supervisor mode (signed space), addresses are sign-extended. Since, the mode is determined by the status register signal, the type of extension is also determined by the signal.

10. Referring to claim 8, Killian has taught a processor as described in claim 7. Killian has further taught that the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment. See column 3, lines 30-31, and column 5, lines 8-19.

11. Referring to claim 9, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag. See column 17, lines 25-27. Note from columns 17-19, that based on the different modes, different address space subsets are used.

12. Referring to claim 11, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference. Recall from previous rejections that a generated 32-bit number is extended to

a 64-bit number in Killian's system. From column 17, line 61, to column 18, line 7, Killian has disclosed that bit 31 of the 64-bit number is checked. If that value is 0, then an address fault has not occurred. However, if that value is 1, then an address exception has occurred. Bit 31, in a sense, represents an overflow bit in that when that bit is set, then the 32-bit application has crossed the 32-bit address space boundary and a fault has occurred. It should be noted that a comparison would inherently be performed to check bit 31. And, this comparison is related to both the original 32-bit address and the extended 64-bit version.

13. Referring to claim 13, Killian has taught a processor as described in claim 7. Killian has further taught that the memory is a cache memory. See column 7, lines 50-52.

14. Referring to claim 14, Killian has taught a processor as described in claim 7. Killian has further taught that the processor is a 64-bit processor. See column 2, lines 16-41, and column 3, lines 30-31. Killian has disclosed that the registers and data path, along with memory addresses, are 64 bits wide. Therefore, Killian has taught a 64-bit processor.

15. Referring to claim 15, Killian has taught a method to confine an application to an address space subset, the method comprising the steps performed by the processor of claim 7. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 7.

16. Referring to claim 17, Killian has taught a method as described in claim 15. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8.

17. Referring to claim 18, Killian has taught a method as described in claim 15. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9.

18. Referring to claim 22, Killian has taught a method as described in claim 15. Furthermore, the processor of claim 11 performs the method of claim 22. Therefore, claim 22 is rejected for the same reasons set forth in the rejection of claim 11.

Response to Arguments

19. Applicant's arguments filed on February 23, 2005, have been fully considered but they are not persuasive. In essence, applicant argues the novelty of the newly added claim language. The examiner asserts that these arguments are responded to in the rejections of the claims above, where the prior art and its relation to the claims are discussed. To summarize, zero extension and sign extension have been taught by Killian and the type of extension to be performed is dependent on a "signal" in the status register which dictates the mode (32/64 and user/kernel/supervisor).

Allowable Subject Matter

20. Claims 12, 23, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 29, 2005

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